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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/498,297	02/04/00	BURSTEIN	A 09464-009001

EXAMINER	
ART UNIT	PAPER NUMBER
2628	4

MMC1/0728

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DATE MAILED: 07/28/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/498,297	Burstein et al.
Examiner	**Group Art Unit**
Rajnikant Patel	2838

☒ Responsive to communication(s) filed on *Feb 4, 2000* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-45* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-45* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hallberg et al. (U.S. Patent # 5,959,442) in combination with Stager et al. (U.S. Patent # 5,777,383). Hallberg et al. discloses claimed invention a voltage regulator (figure 2) having an input terminal (figure 2, item VIN) and output terminal (figure 2, item VOUT),a filter disposed to provide a substantially DC voltage at the output terminal (figure 2, item 112), and a control circuit to control the power switch to maintain the DC voltage substantially constant (figure 2, item 114). However Hallberg et al. does not disclose the technique of packaging voltage regulator on a printed circuit board; a substrate mounted on the printed circuit board; a first flip-chip type integrated circuit chip mounted on the substrate, the first integrated circuit chip including a first power switch fabricated therein to alternately coupled and decoupled the input terminal to output terminal. Stager et al. teaches the technique of packaging voltage regulator on a printed circuit

board; a substrate mounted on the printed circuit board; a first flip-chip type integrated circuit chip mounted on the substrate, the first integrated circuit chip including a first power switch fabricated therein to alternately coupled and decoupled the input terminal to output terminal (figure 1, 2 and column 2, line 45-65). It would have been obvious to one having a ordinary skill in the art at the time the invention made to modify Hallberg et al.'s voltage regulators by utilizing the technique of packaging voltage regulator on printed circuit board as taught by Stager et al. for the purpose of providing a highly efficience reliable voltage regulator.

In regards to claims 2-7, Hallberg et al. in combination with Stager et al. discloses the power switch and filter form a buck converter topology (Hallberg et al.'s patent column 1, 15-20), the integrated circuit chip is mounted on the substrate with array of solder bumps (Stager et al.'s patent column 3, line 60), p-type and n-type region (Hallberg et al.'s patent, figure 2, item 120 and 122)

3. Claims 8-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hallberg et al. in combination with Stager et al. and further in combination with Honn et al. (U.S. Patent # 5,777,383) .

Hallberg et al. in combination with Stager et al. discloses claimed invention as explained in claims 1-7, above. The 8-45 claims are directed to a different methods of fabricating semiconductor chips on a different packages and interconnect the packages which is very well known in the art some of

that techniques are disclosed by Hallberg et al. in combination with Stager et al. and further in combination with Honn et al. (Honn et al.'s patent figure 1A and 1B)

4. Any inquiry concerning this communications or earlier from the examiner should be directed to Raj. Patel whose telephone number is (703) 305-7042. Any inquiry of a general nature or relating to the status of application should be directed to the Group receptionist whose telephone number is (703) 308-1782.

R. B. Patel

July 26, 2000